

CONTENT	SHEET
Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals/ Power/ GND	3-5
Intel Bearlake - FSB, PCIE, DMI, VGA, MSIC	6
Intel Bearlake - Memory	7
Intel Bearlake - Power / GND	8-9
ICH9 - PCI, USB, DMI, PCIE	10
ICH9 - Host, DMI, SATA, Audio, SPI, RTC, MSIC	11
ICH9 - Power, GND	12
DDR3 & DDR2 Chanel-A / Chanel-B	13-14
Clock Gen ICS9LPRS906	15
Super I/O Fintek F71882	16
PS2 / COM / VGA Port	17
SATA / e-SATA / FAN Control	18
LAN Realtek RTL8111(PCIE)	19
Audio Codec ALC888	20
PCIE x16, x1 & Bus Switch	21
PCI Slot 1 & 2	22
Marvell 88SE6111 PCIE to IDE/ SATA	23
USB Connectors	24
IEEE1394 VT6308	25
System Power/ACPI Controller UPI	26
DDR / NB-Core Switching Power	27
VRD 11 - ISL6322CR(3Phases)	28
ATX Power-Con. / F_Panel	29
Manual & Option Parts	30
Power Delivery	31
Reset & PWROK map	32
GPIO Setting & PCI Routing / Revision History	33-34

MS-7365

ATX Version: 0A

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q/G/P (G33, P35, Q35/33North Bridge)
Intel ICH9 (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111 (PCIE)
HD Audio Codec -- ALC888
1394 Controller -- VT6308 (2-port)
PCIE to PATA/SATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-III*2 DDR-II *2

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 3
PCI SLOT * 2

PWM: Intersil ISL6322CR (3Phases)

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD		Cfg-7365-STD	601-7365-A10
A		Cfg-7365-A	601-7365-B10

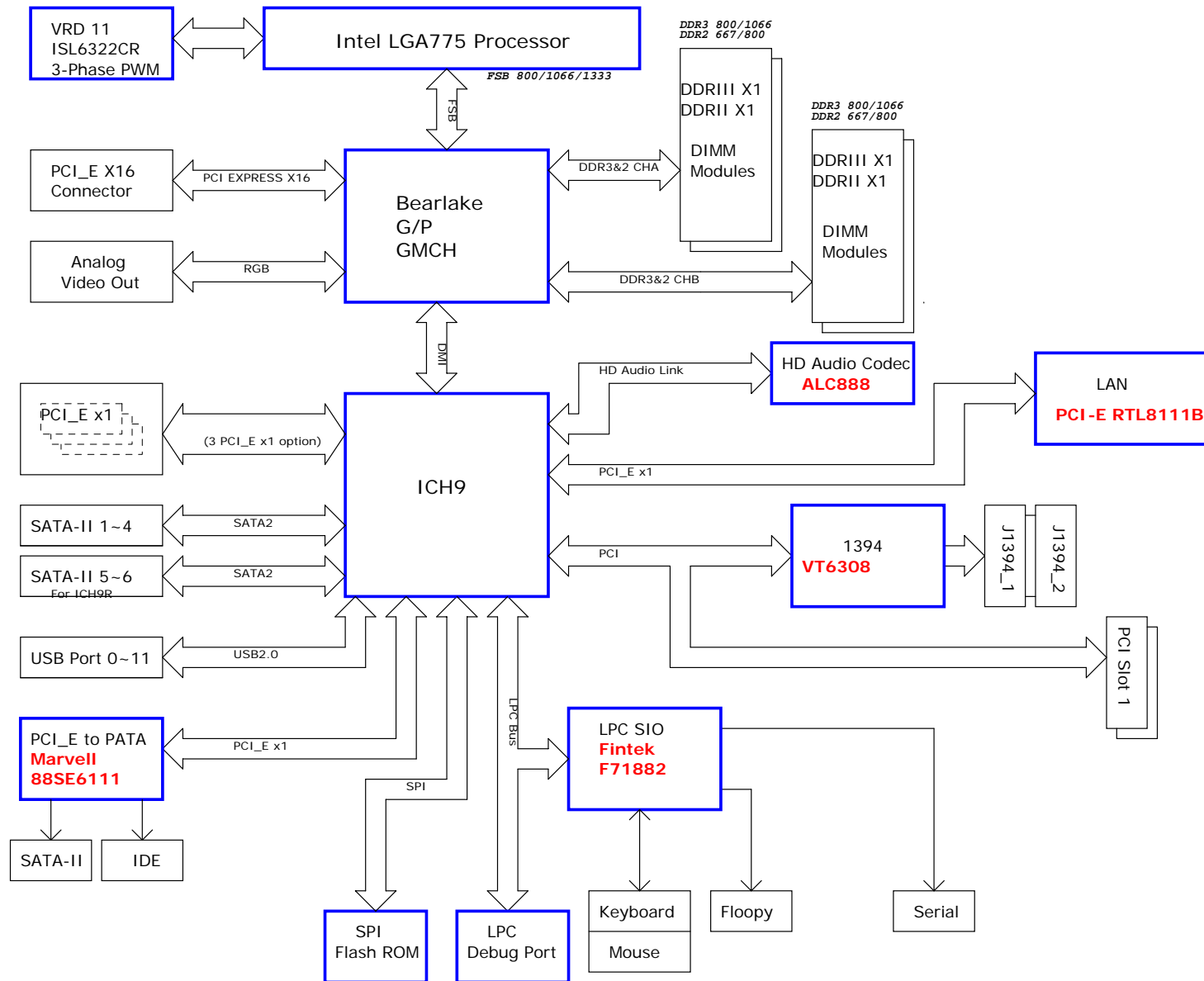


MICRO-STAR INT'L CO.,LTD

MS-7365

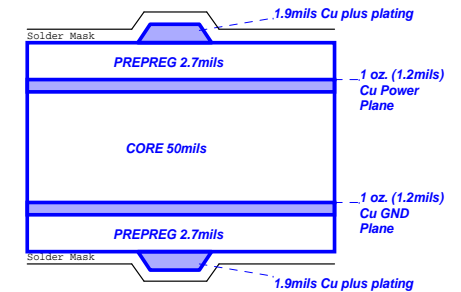
Size Custom	Document Description COVER SHEET	Rev 0A
Date: Monday, April 02, 2007	Sheet 1 of 34	

Block Diagram

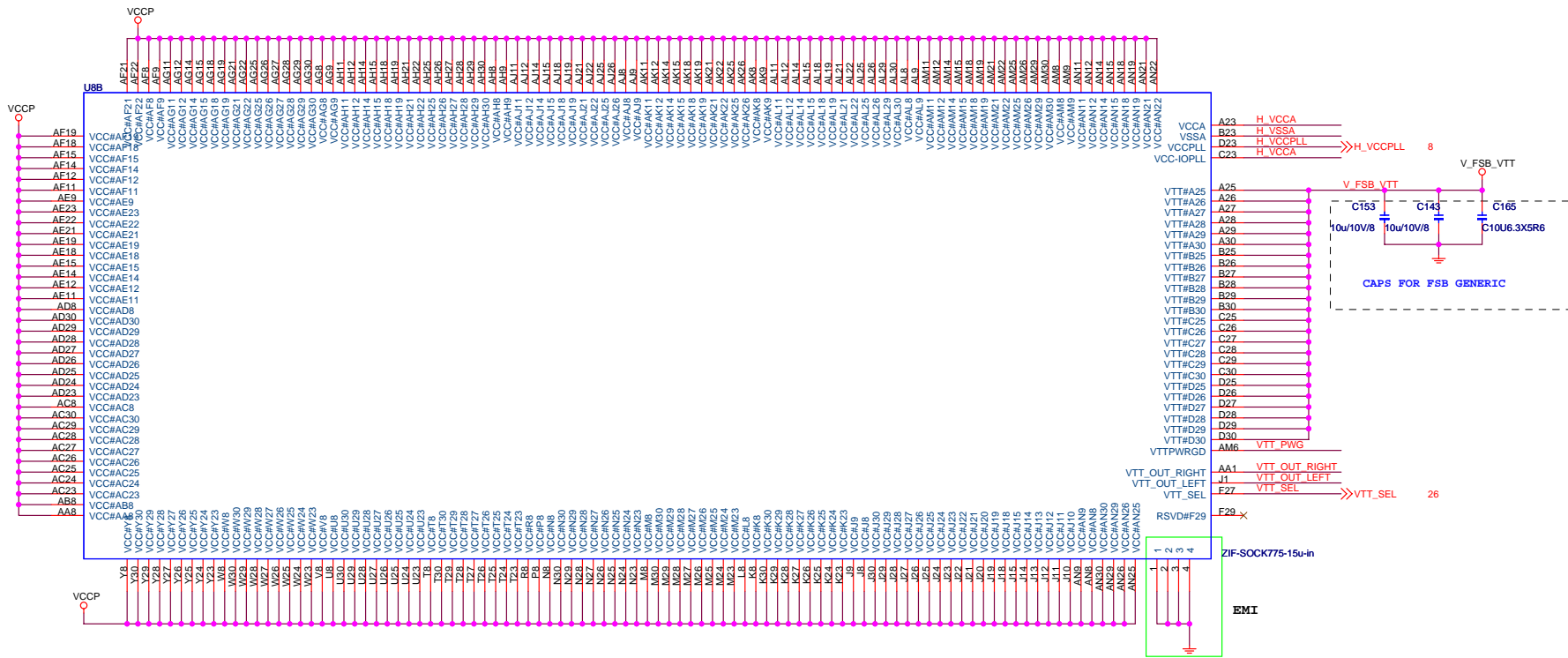


Board Stack-up

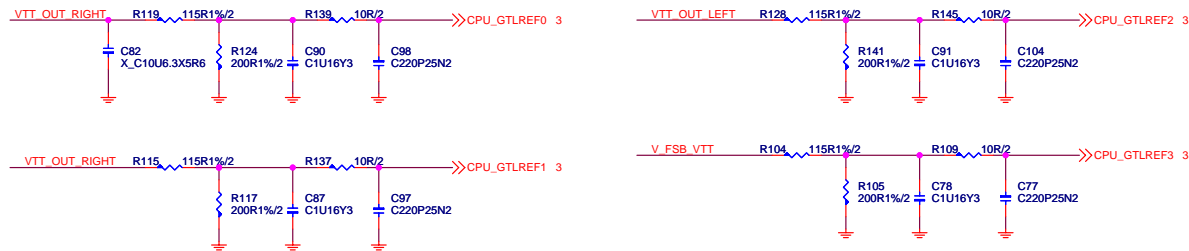
(1080 Prepreg Considerations)



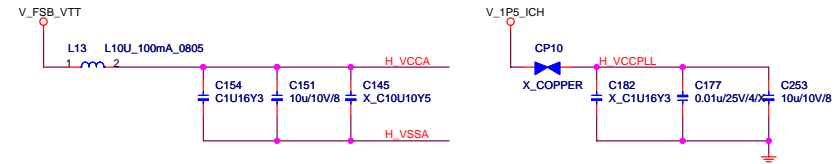
Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15



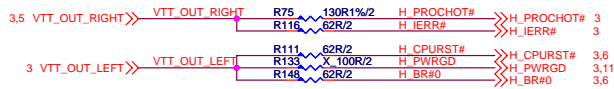
*GTLREF VOLTAGE SHOULD BE
 0.67 * VTT = 0.8V (At VTT=1.2V)



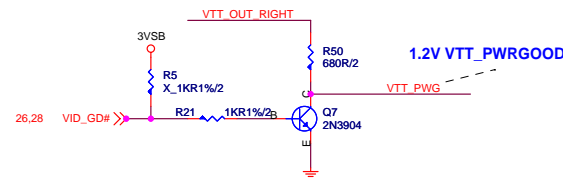
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
 *TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT PWRGOOD

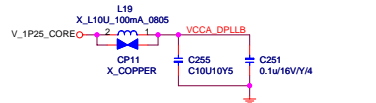
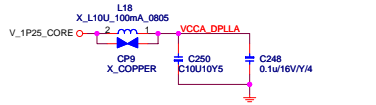
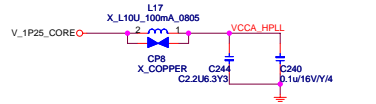
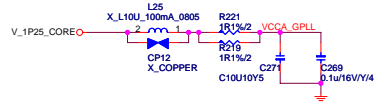
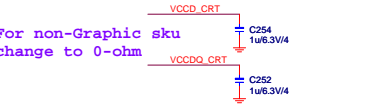


MICRO-STAR INT'L CO.,LTD			
MS-7365			
Size	Document Description	Rev	
Custom	LGA775 - Power	0A	
Date: Monday, April 02, 2007	Sheet	4	of 34

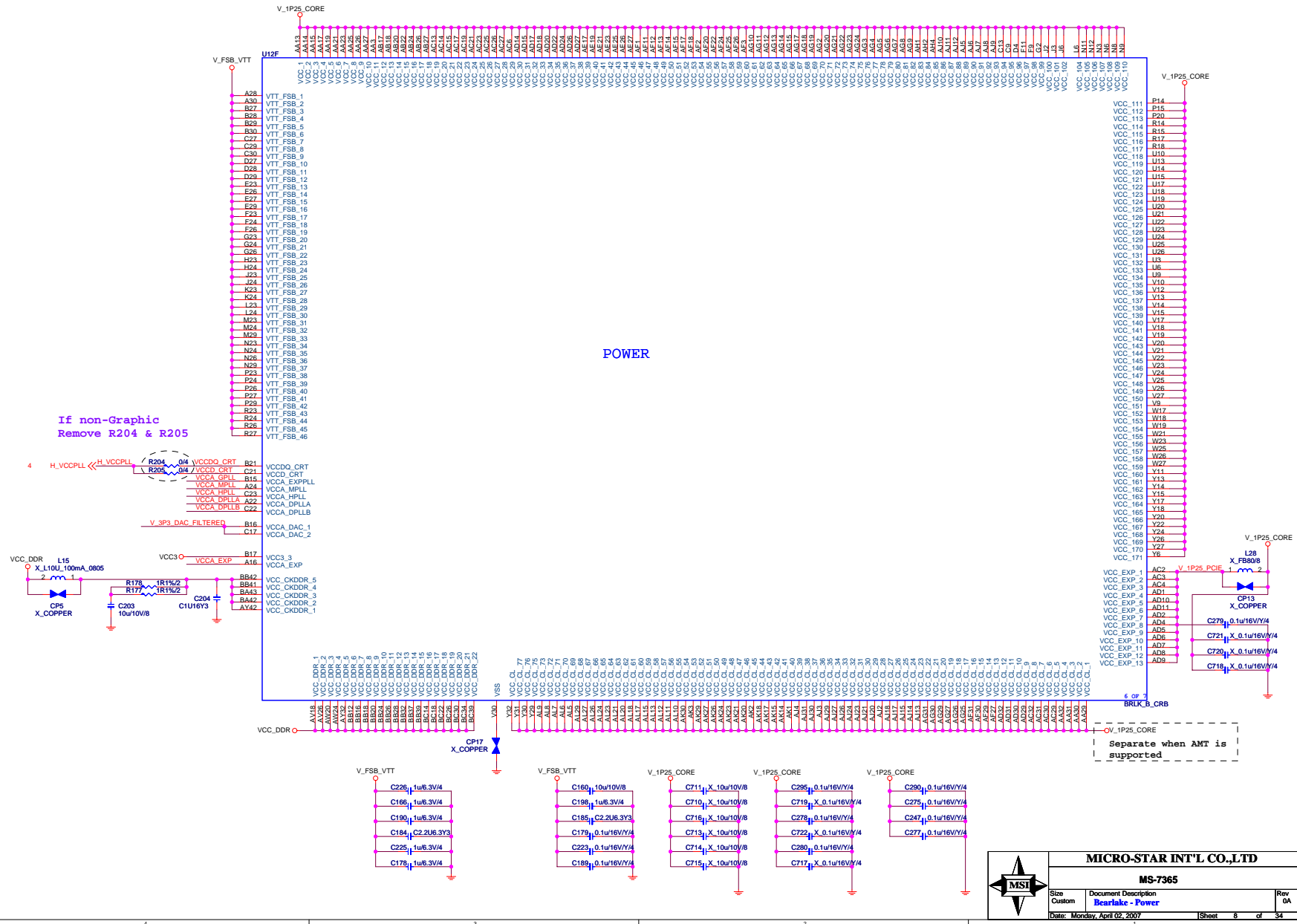
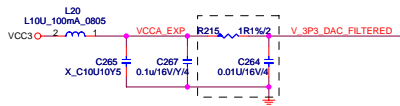
NB POWER

For non-Graphic sku
change to 0-ohm

For non-Graphic sku
change to 0-ohm



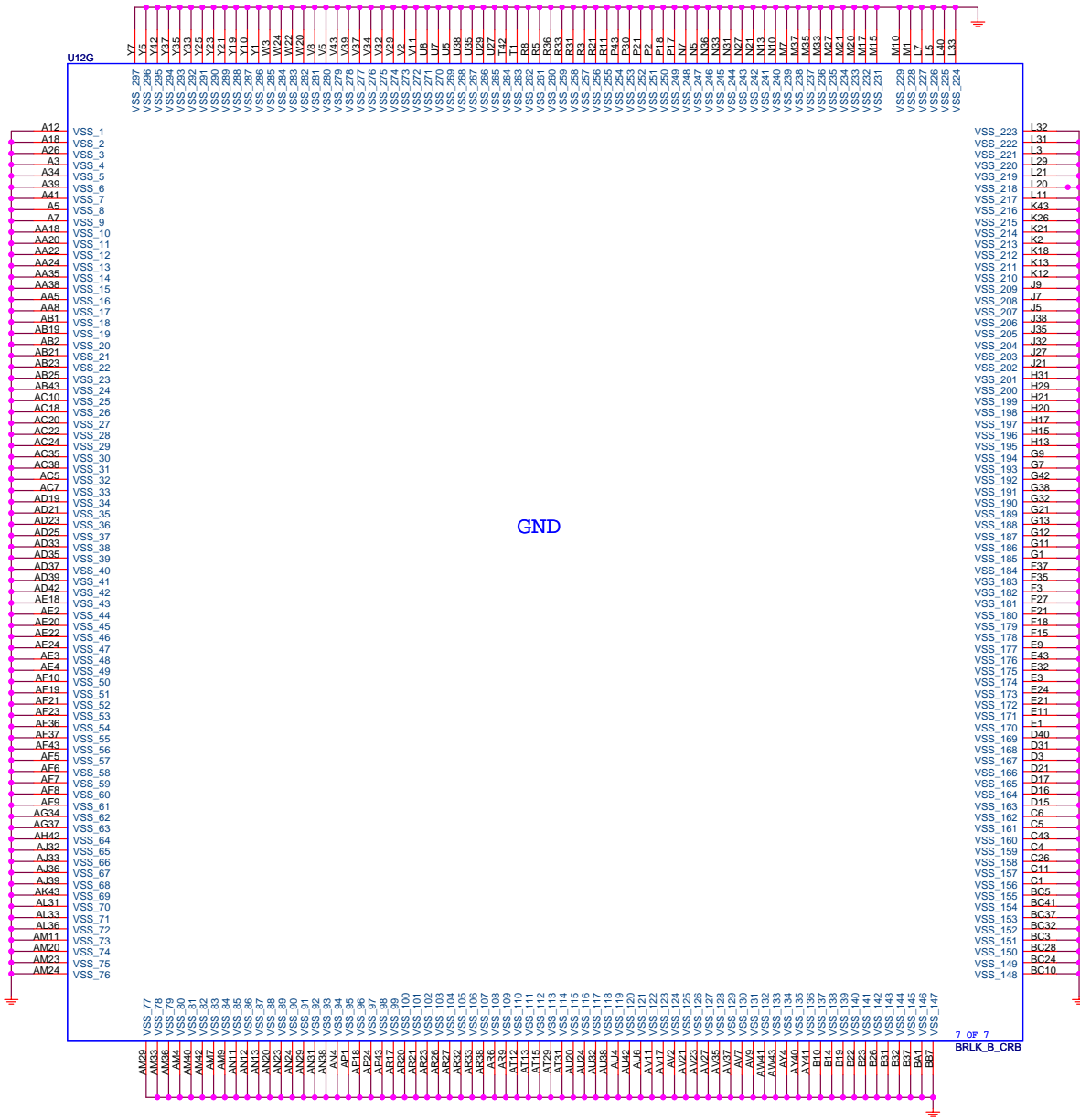
For non-Graphic SKU VCCA_R1
Remove R215

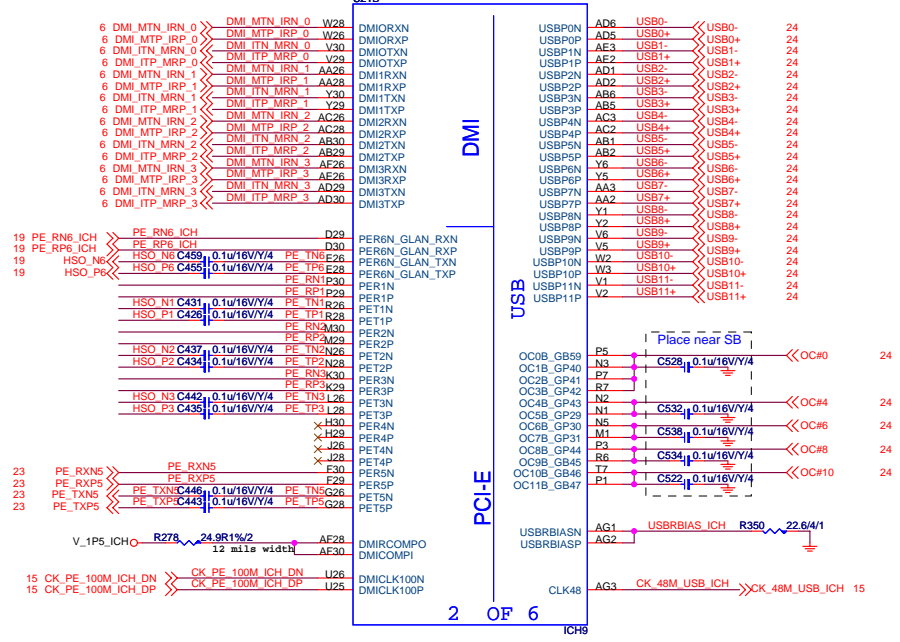
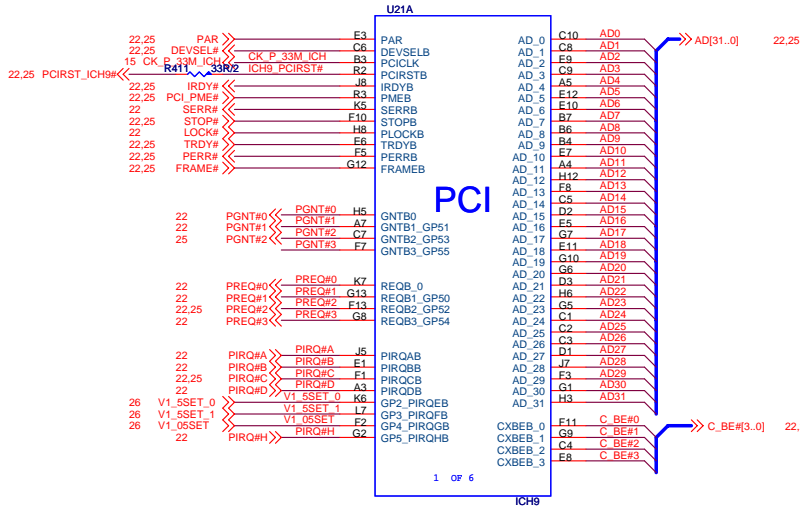


MICRO-STAR INT'L CO.,LTD

MS-7365

Size Custom	Document Description Bearlake - Power	Rev 0A
Date: Monday, April 02, 2007		Sheet 8 of 34





SB STRAPPING RESISTOR

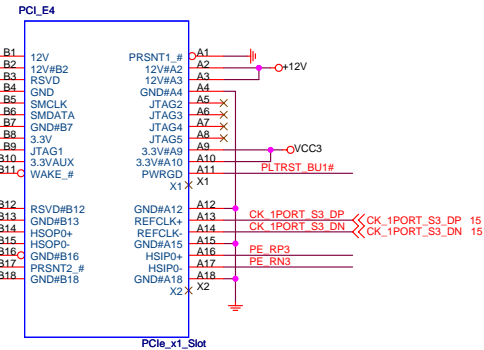
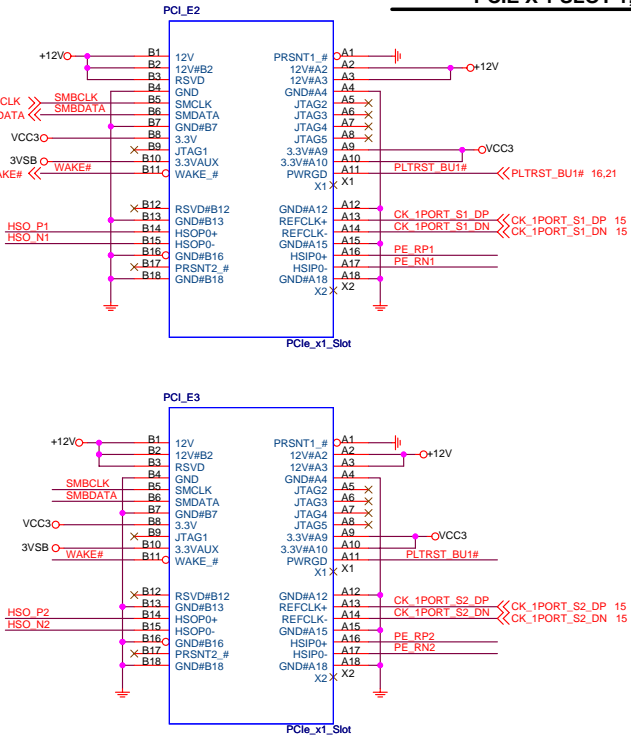


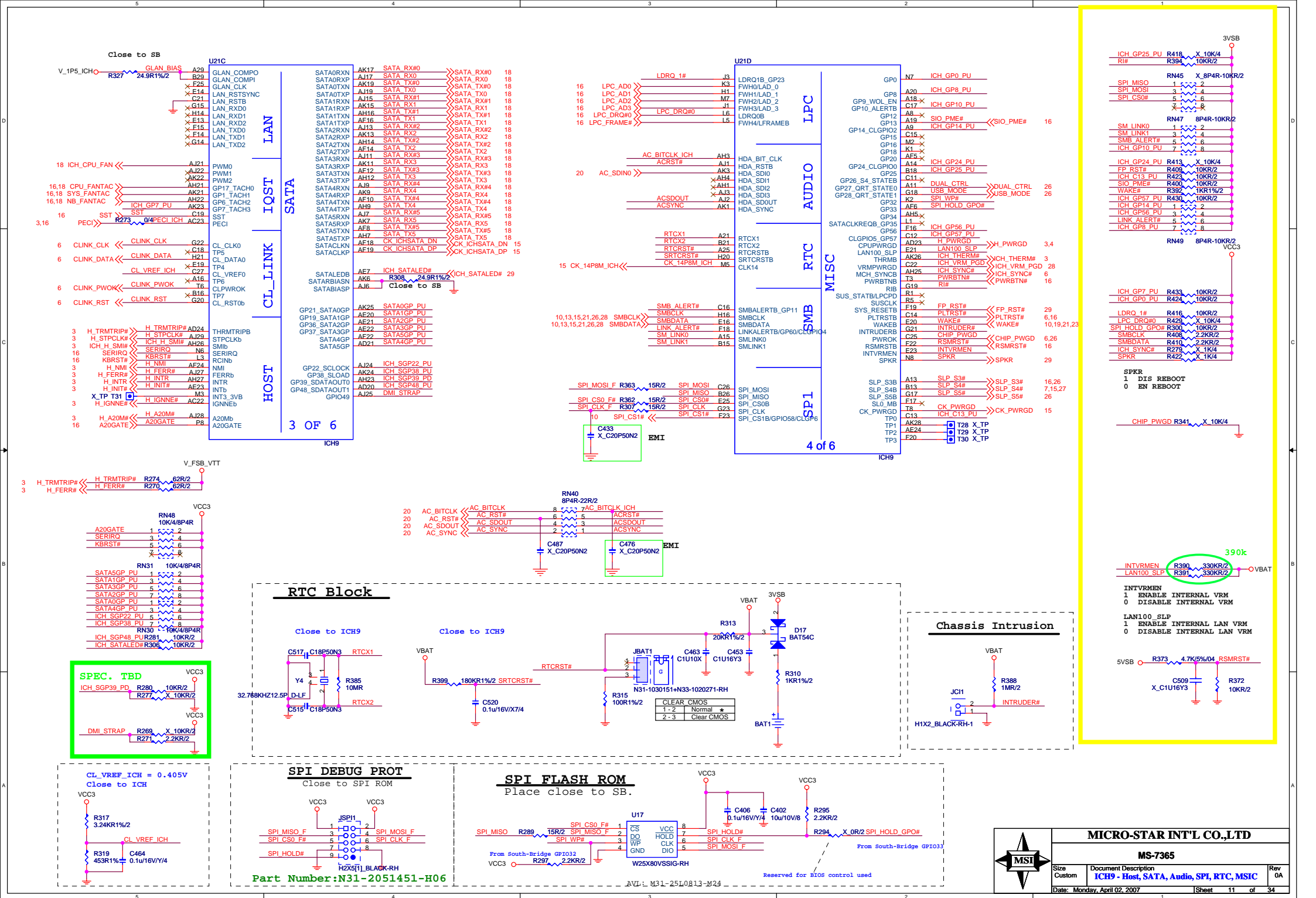
BOOT DEVICE	GNT#0	SPI_CS#1
FWH	1	1
SPI	0	1
PCI	1	0



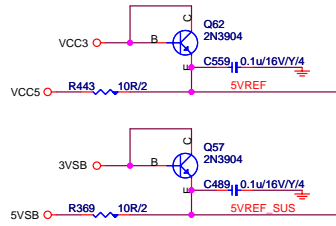
SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

PCIE X1 SLOT 1,2,3

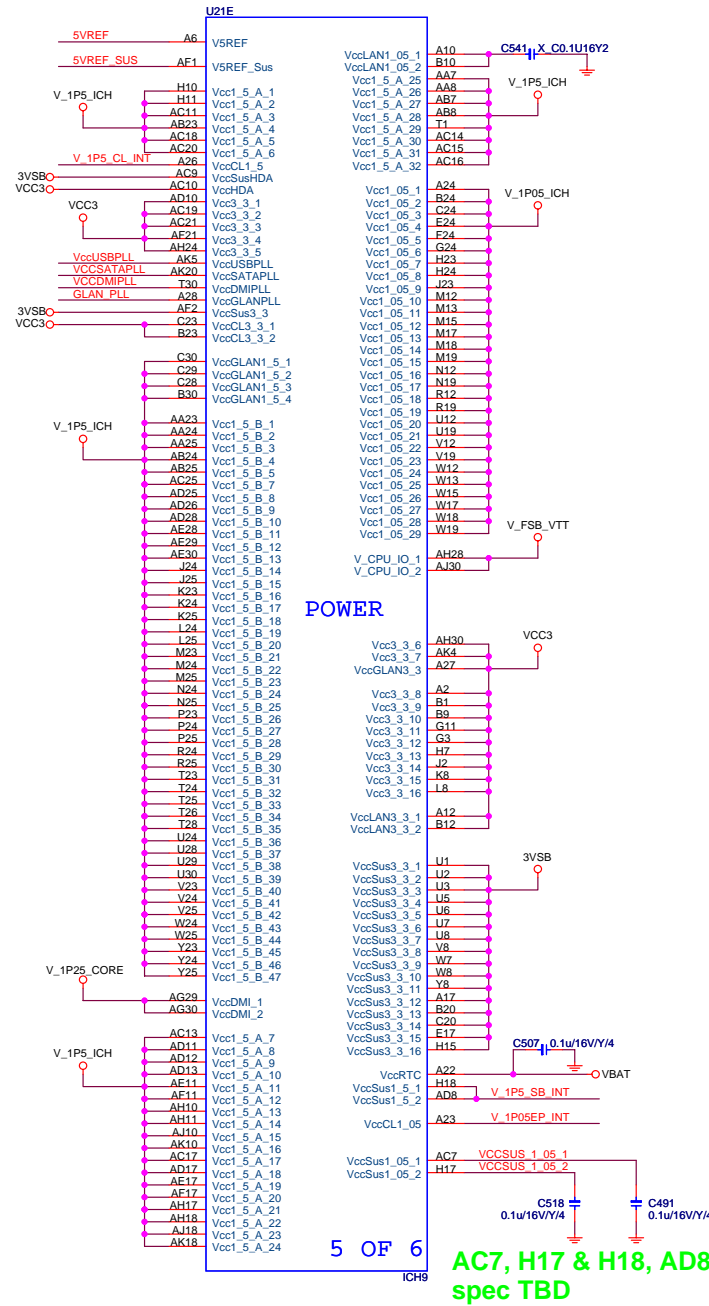
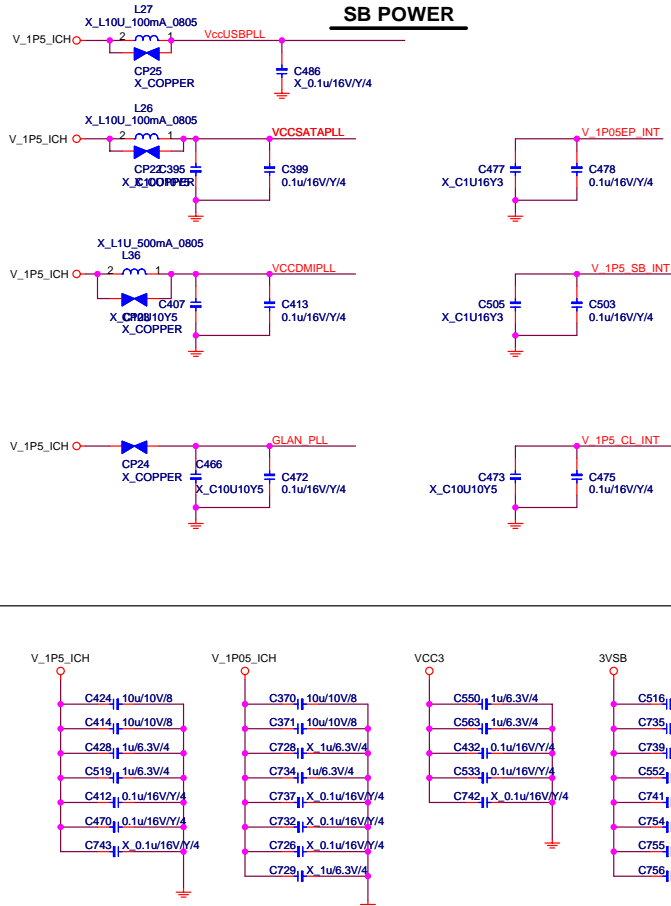




5VREF & 5VREF_SUS Sequencing Circuit

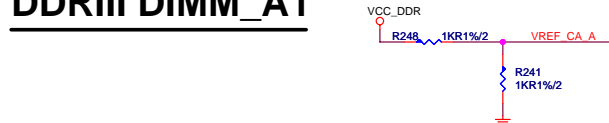


SB POWER



MICRO-STAR INT'L CO.,LTD		
MS-7365		
Size	Document Description	Rev
Custom	ICH9 - Power, GND	0A
Date: Monday, April 02, 2007		Sheet 12 of 34

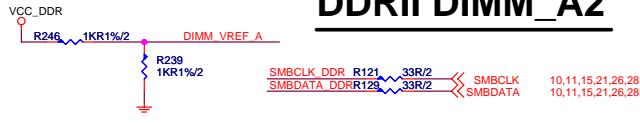
DDRIII DIMM_A1



DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DDR3_DET# → DDR3_DET# 14,27

DDRII DIMM_A2



DDR2_DET# → DDR2_DET# 14,27

ADDRESS: 001
0xA2

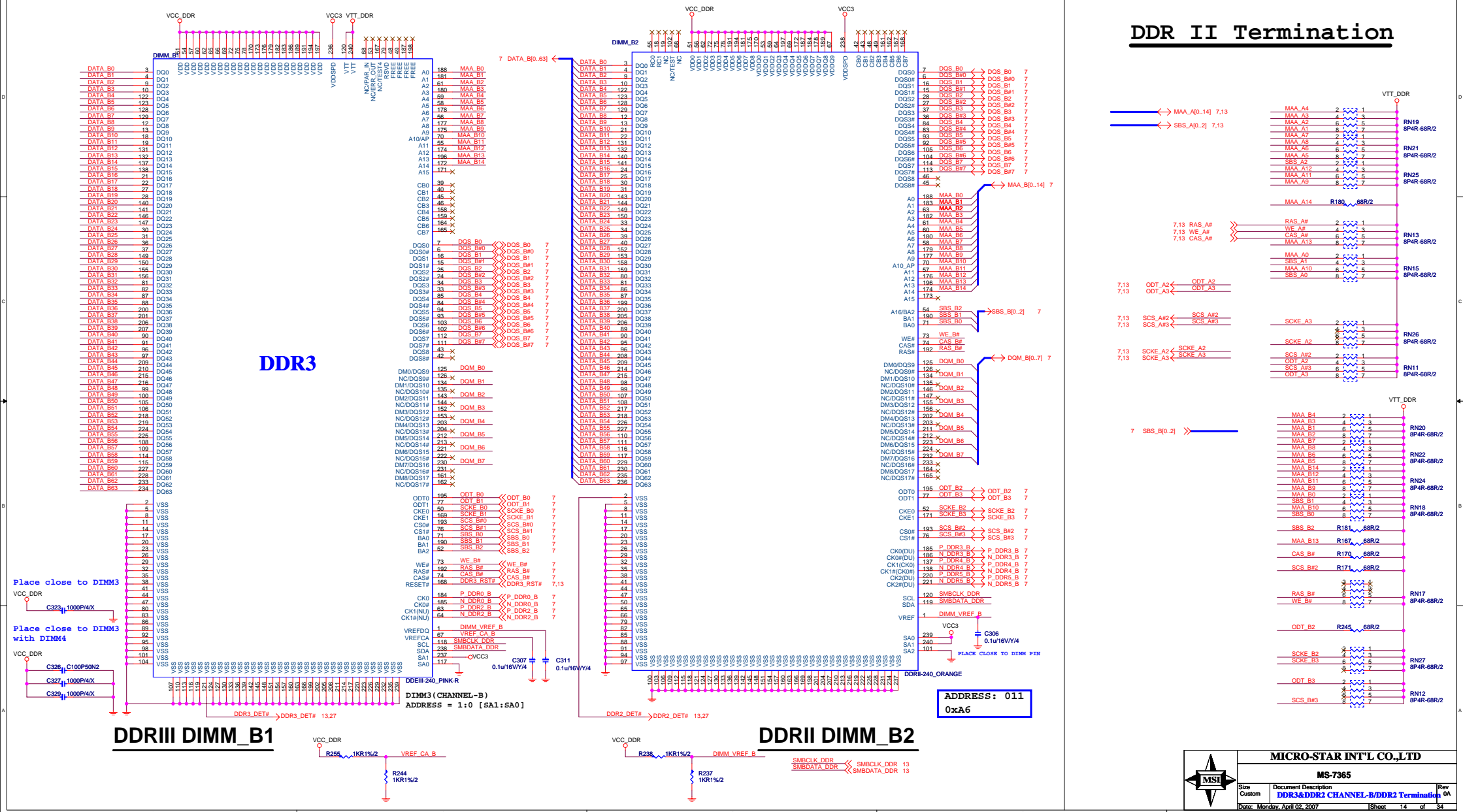


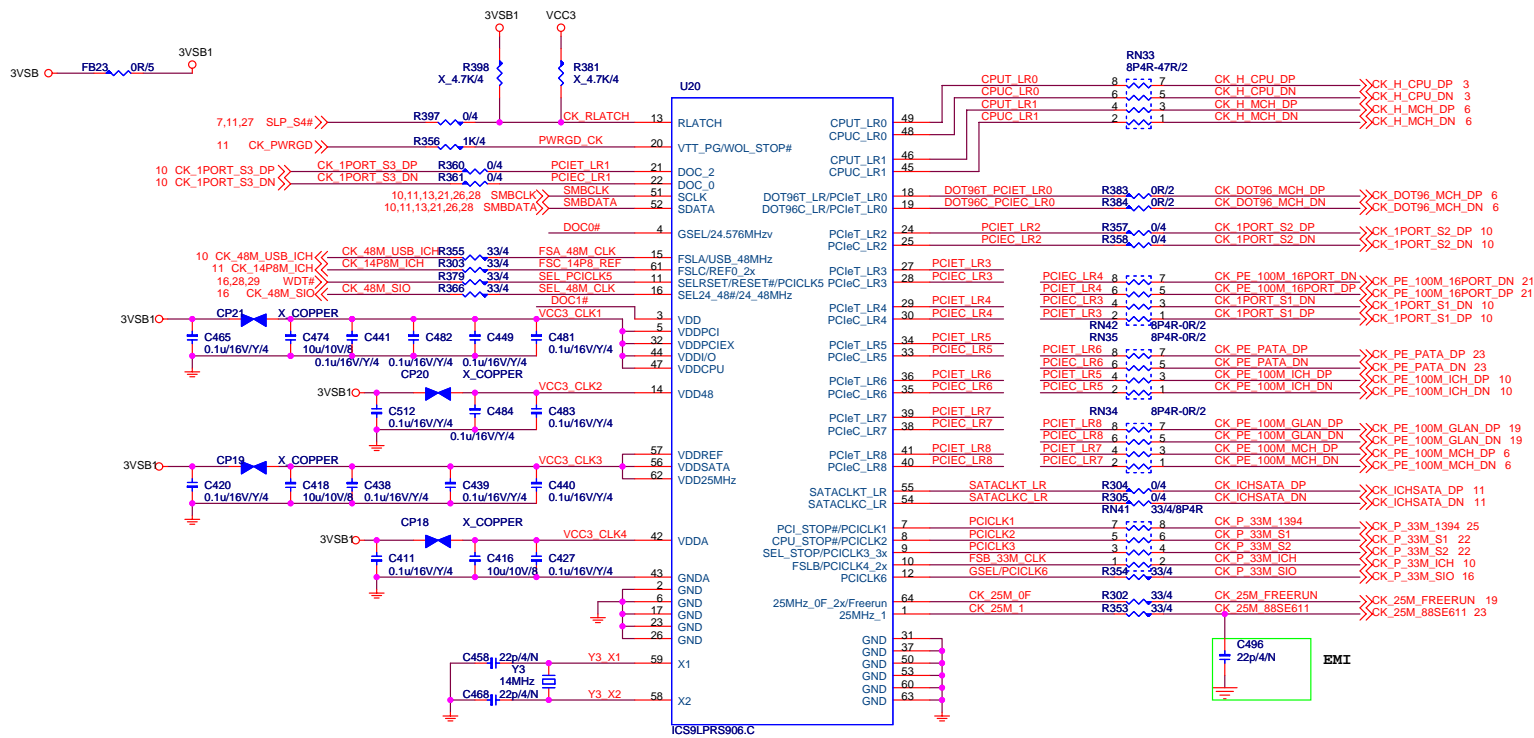
MICRO-STAR INT'L CO.,LTD

MS-7365

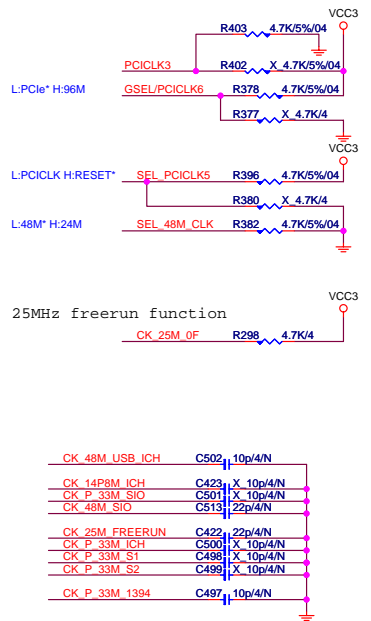
Size	Document Description	Rev
Custom	DDR3&DDR2 CHANNEL-A	0A
Date: Monday, April 02, 2007	Sheet 13 of 34	

DDR II Termination



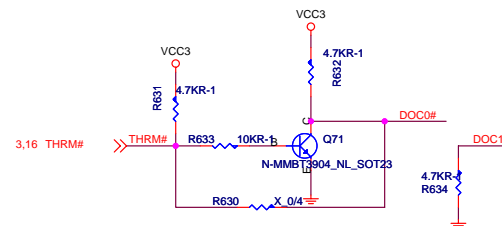
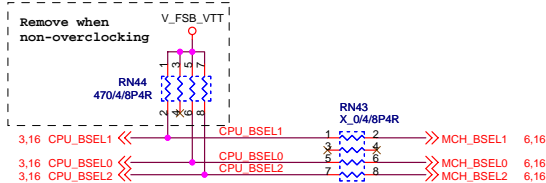


CLOCK GEN STRAPPING



BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz (1066)
0 0 1	133 MHz (533)
0 1 0	200 MHz (800)

CPU_BSEL0	R351	1K/4	FSA 48M_CLK
CPU_BSEL1	R352	1K/4	FSB 33M_CLK
CPU_BSEL2	R296	1K/4	FSC 14P8_REF



DOC#0	DOC#1	State
0	0	Normal
1	0	By BIOS

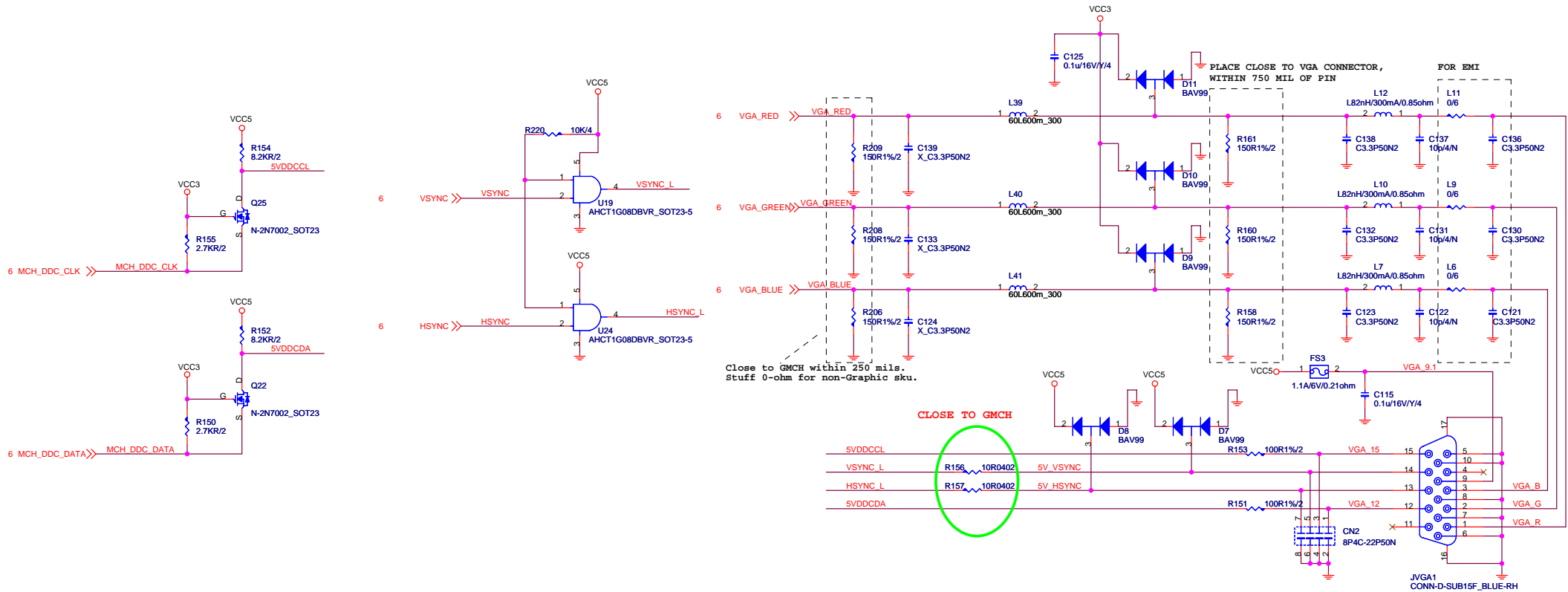


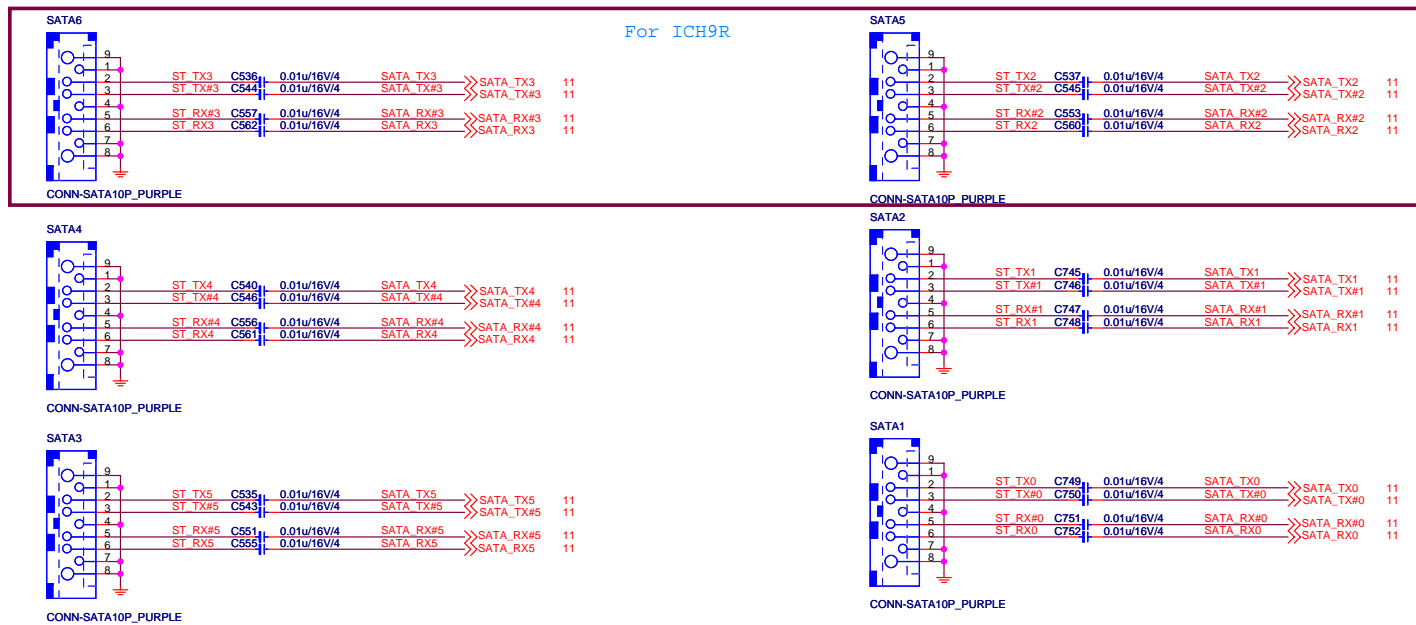
MICRO-STAR INT'L CO.,LTD

MS-7365

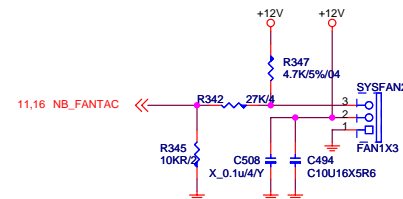
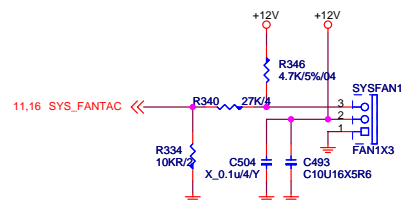
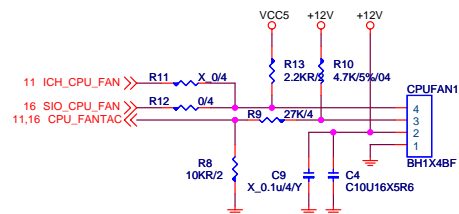
Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS906	0A
Date: Monday, April 02, 2007	Sheet 15 of 33	

Video Connector

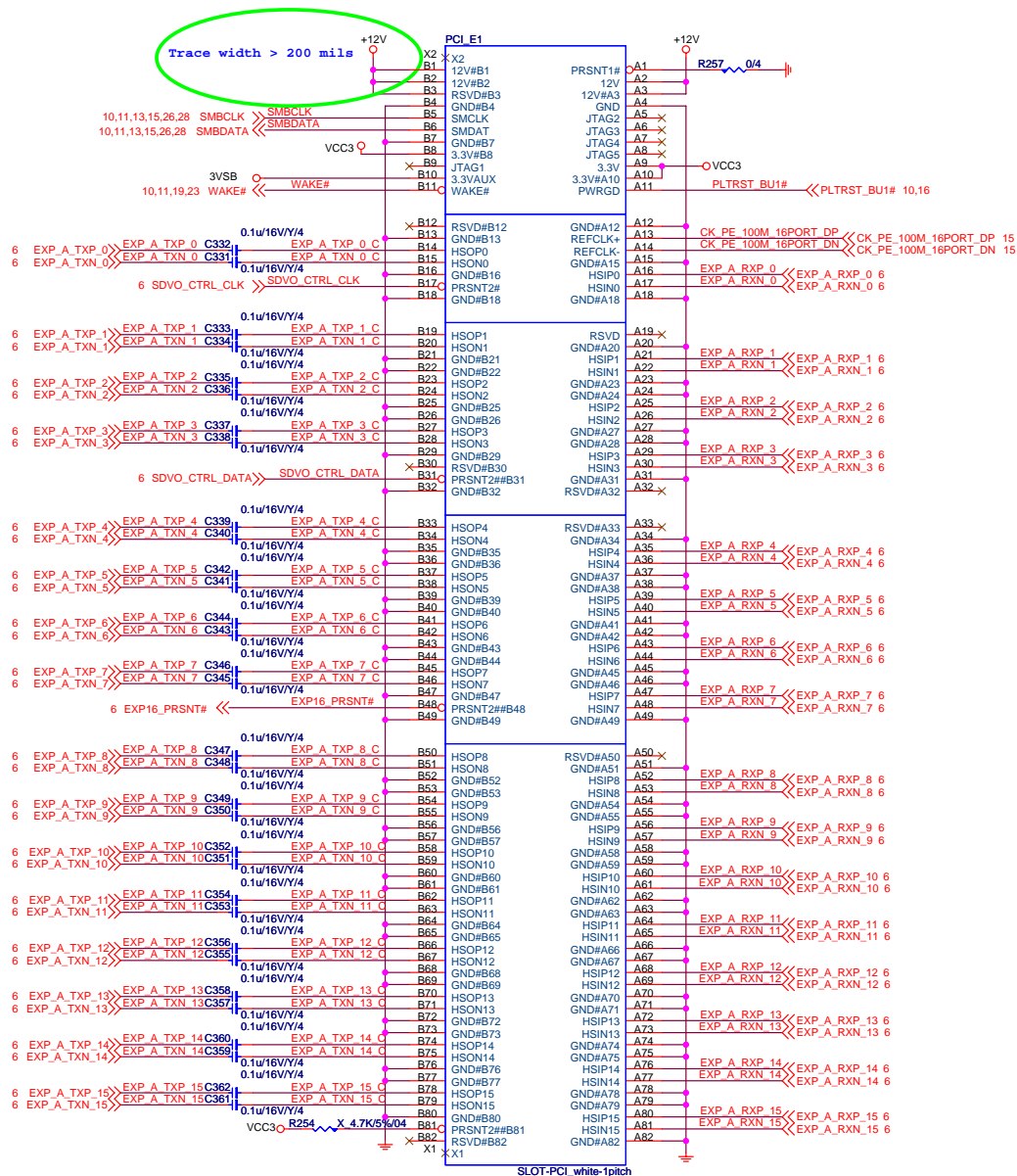




FAN-COUNTROL CIRCUIT



PCI_Express X16 slot

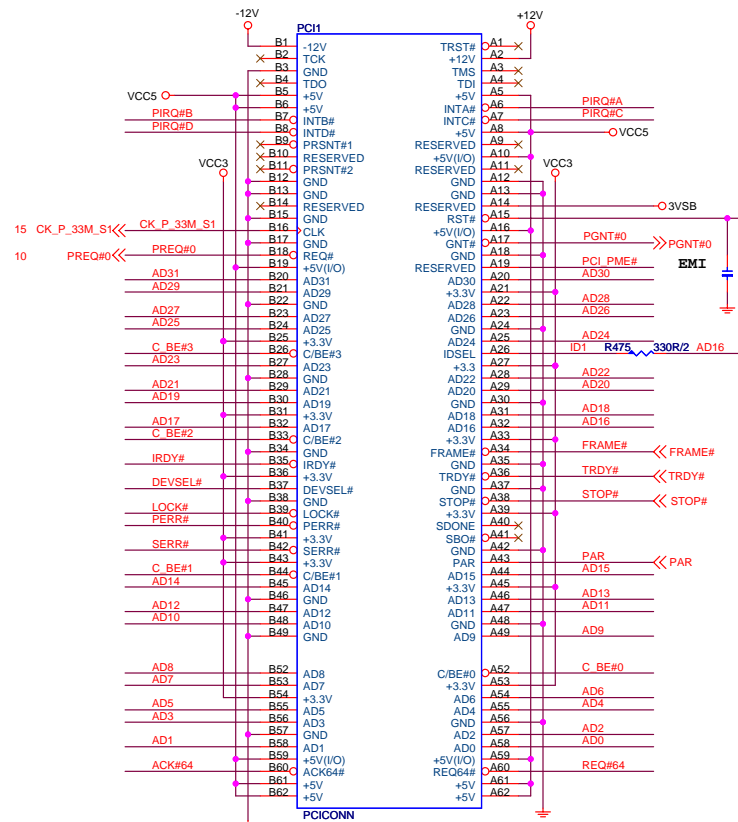


MICRO-STAR INT'L CO.,LTD

MS-7365

Size	Document Description	Rev
Custom	PCIe x16, x4, x1 & Bus Switch	0A
Date:	Monday, April 02, 2007	Sheet 21 of 34

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16

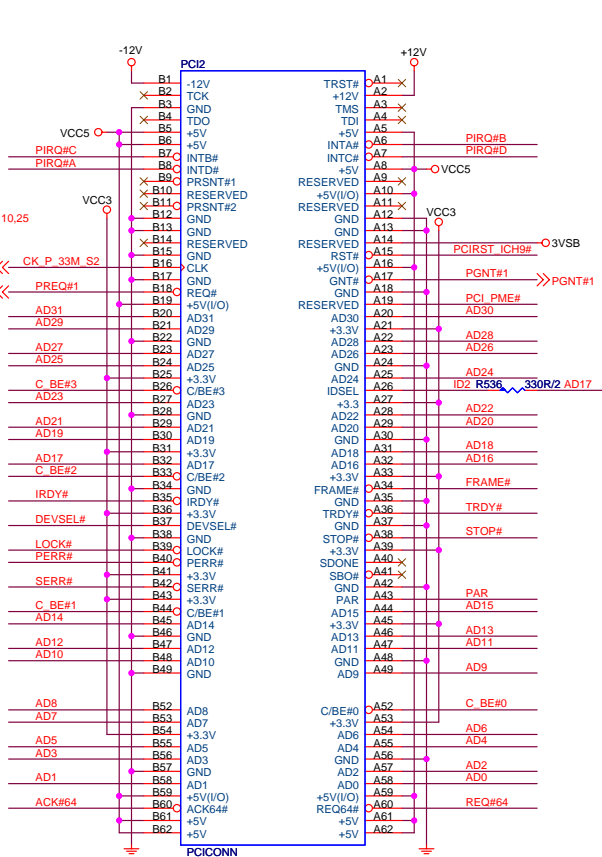
MASTER = PREQ#0

PIRQ#A

10,25 AD[31:0] << AD[31:0]

10,25 C_BE#[3:0] << C_BE#[3:0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

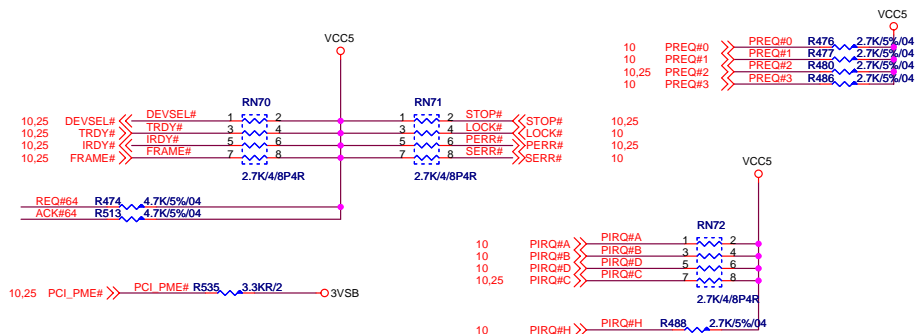


IDSEL = AD17

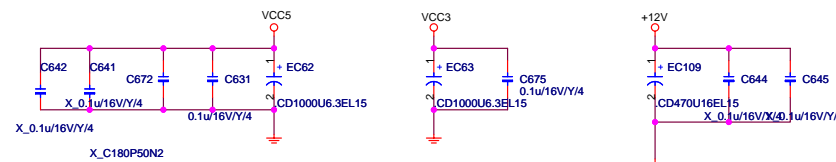
MASTER = PREQ#1

PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



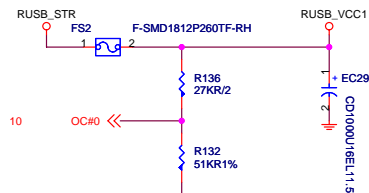
MICRO-STAR INT'L CO.,LTD

MS-7365

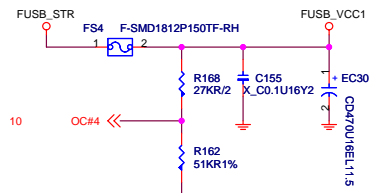
Size	Document Description	Rev
Custom	PCI Slot 1 & 2	0A
Date: Monday, April 02, 2007	Sheet 22 of 34	

Rear USB Connector

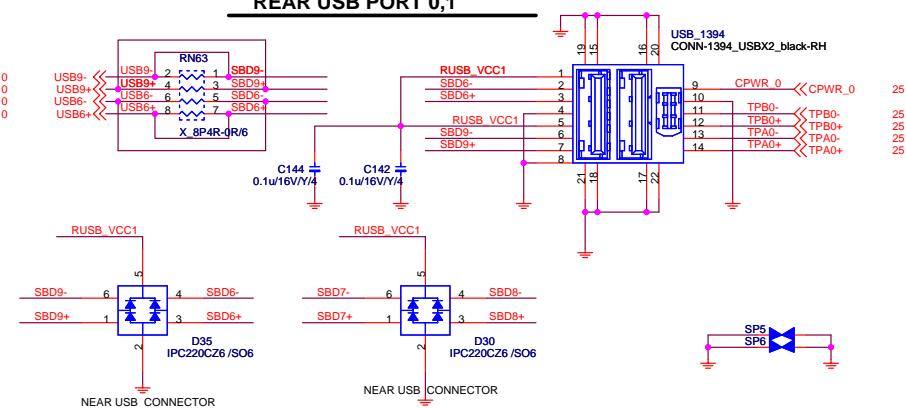
USB POWER FOR PORT 0,1 NEAR CONNECTOR



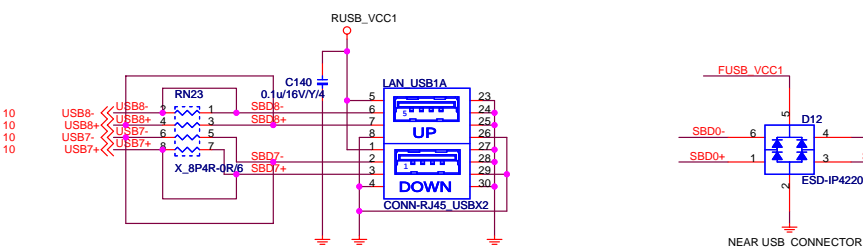
USB POWER FOR PORT 6,7,8,9 NEAR CONNECTOR



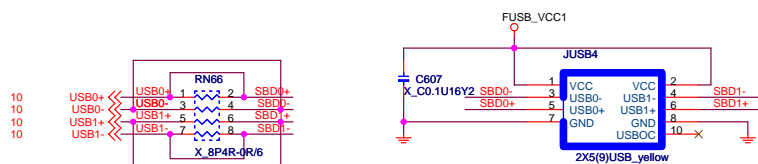
REAR USB PORT 0,1



REAR USB PORT 2,3 (With LAN)

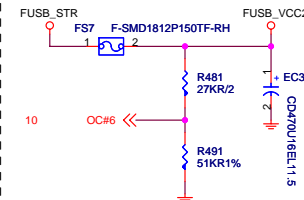


FRONT USB PORT 0,1

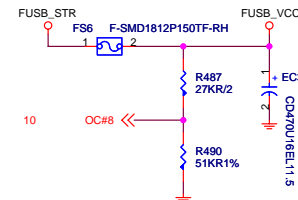


Front USB Connector

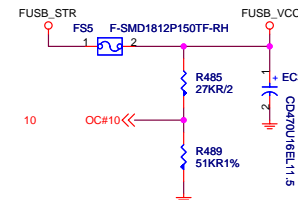
USB POWER FOR PORT 6,7 NEAR CONNECTOR



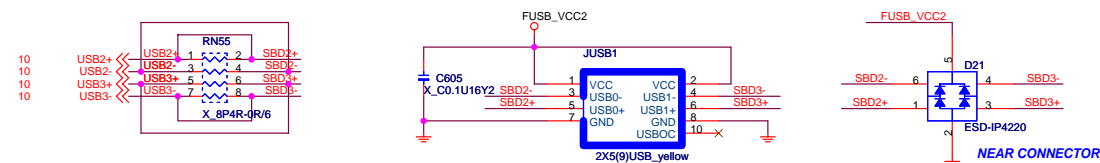
USB POWER FOR PORT 6,7 NEAR CONNECTOR



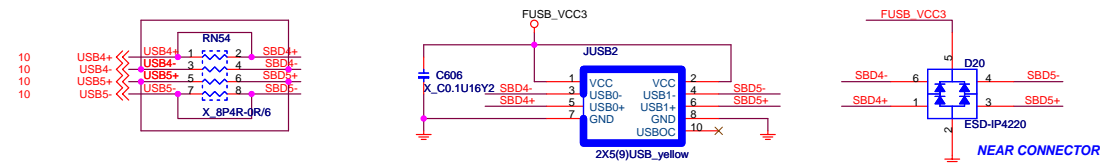
USB POWER FOR PORT 6,7 NEAR CONNECTOR



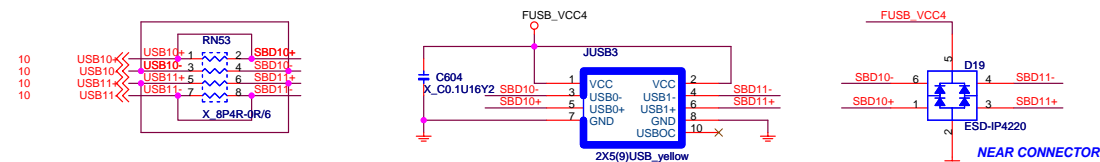
FRONT USB PORT 2,3




FRONT USB PORT 4,5



FRONT USB PORT 10,11

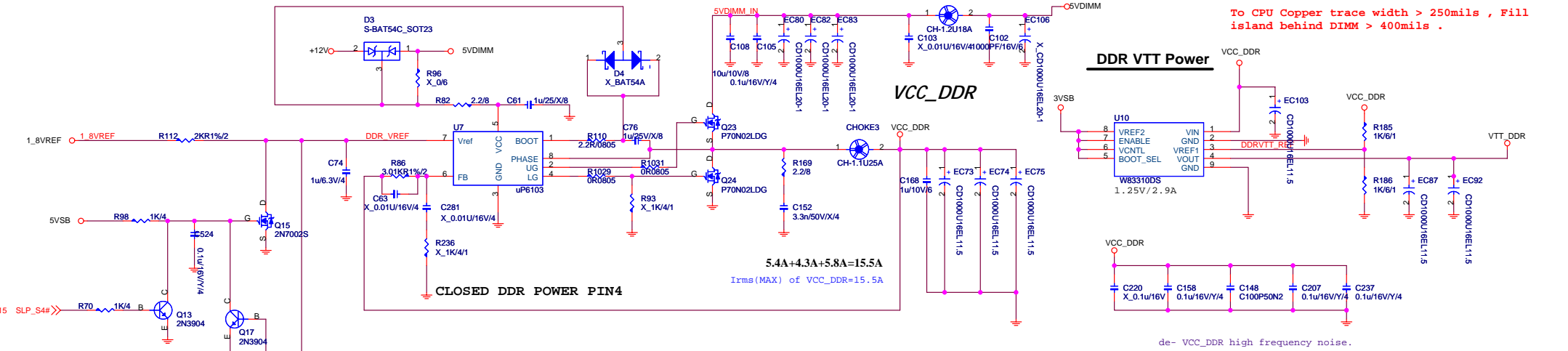


			
MICRO-STAR INT'L CO.,LTD			
MS-7365			
Size	Document Description	Rev	
Custom	USB Connector	0A	
Date: Monday, April 02, 2007	Sheet 24 of 34		

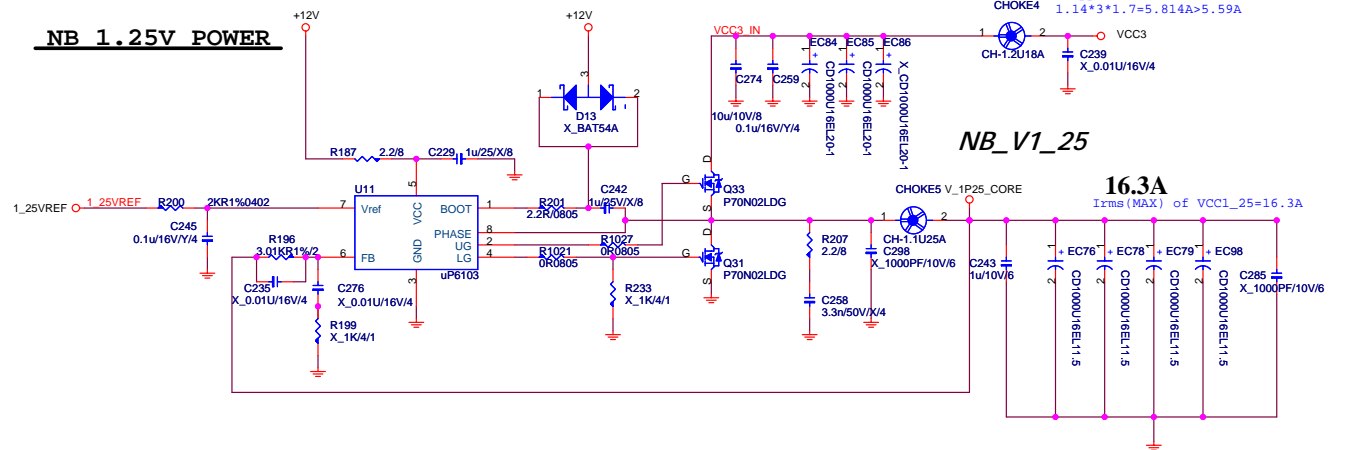
DDRII/1.8V & DDRIII/1.5V POWER

$$\text{Irripple}=15.5 \times 1.8 / (5 \times 0.8) = 6.98 \text{A}$$

$$2.22 \times 3 \times 1.7 = 11.322 \text{A} > 6.98 \text{A}$$



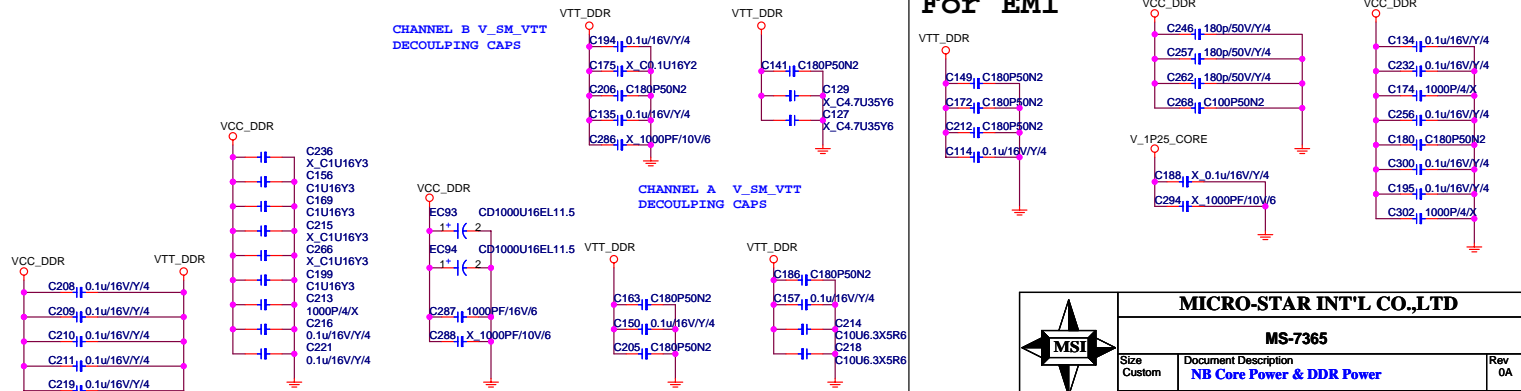
NB 1.25V POWER

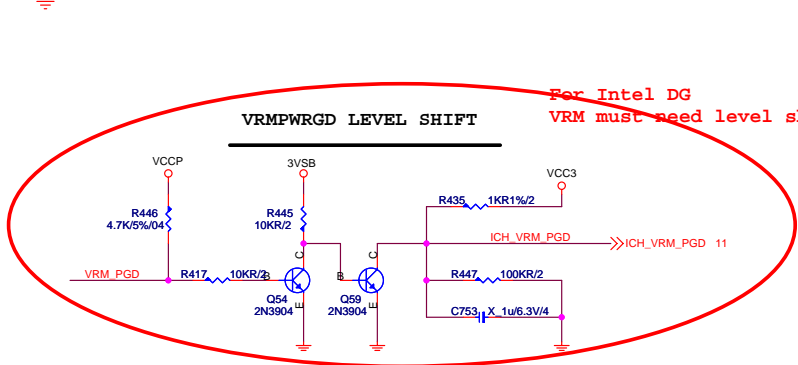
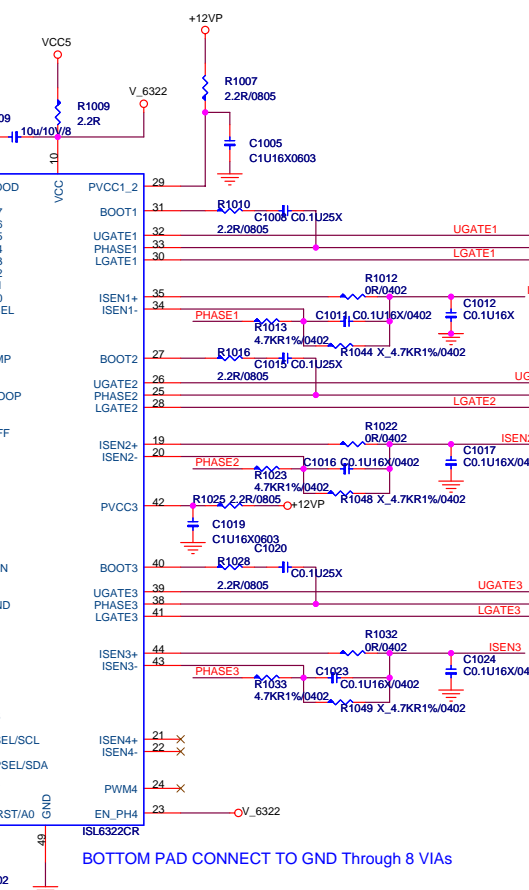
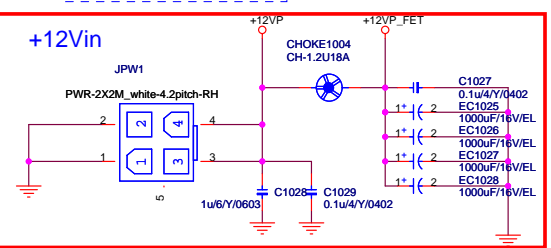
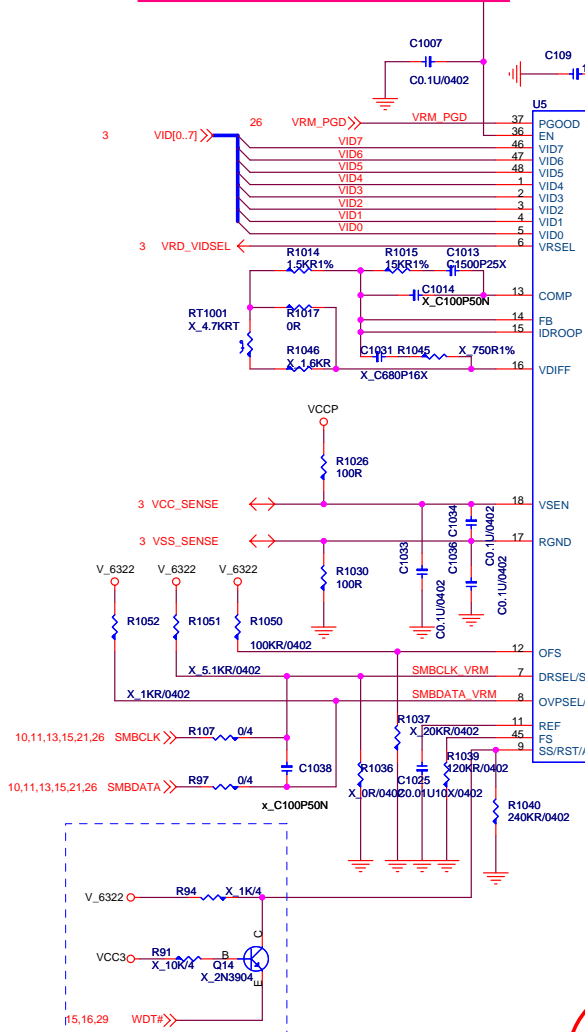
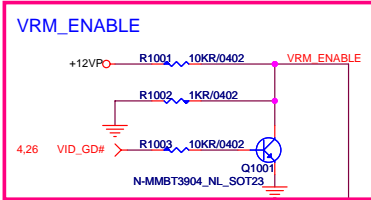


DDR3_DET#	MCH_MTYPE	DDR3	DDR2	DDRVREF
0	0	On	Off	1.5V
1	1	Off	On	1.8V

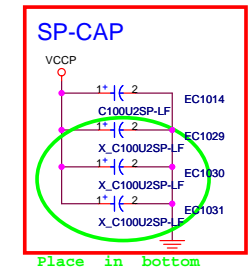
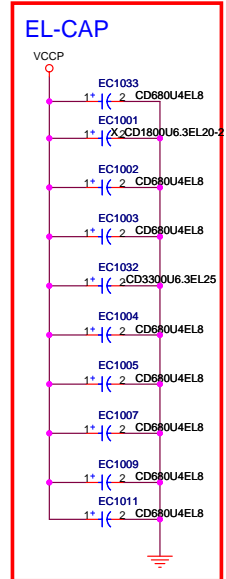
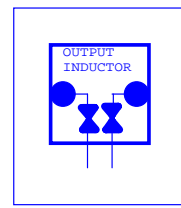
DDR2_DET#	MCH_MTYPE	DDR3	DDR2	DDRVREF
1	0	On	Off	1.5V
0	1	Off	On	1.8V

For EMI



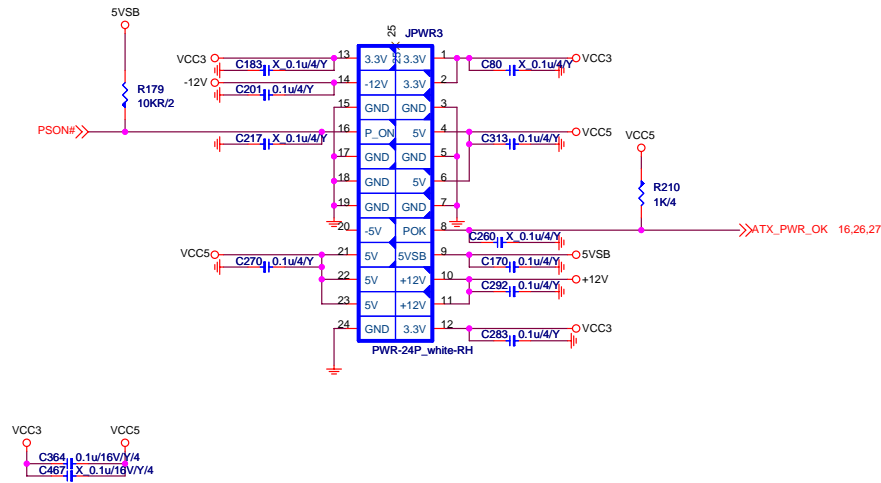


For Intel DG
VRM must need level shift

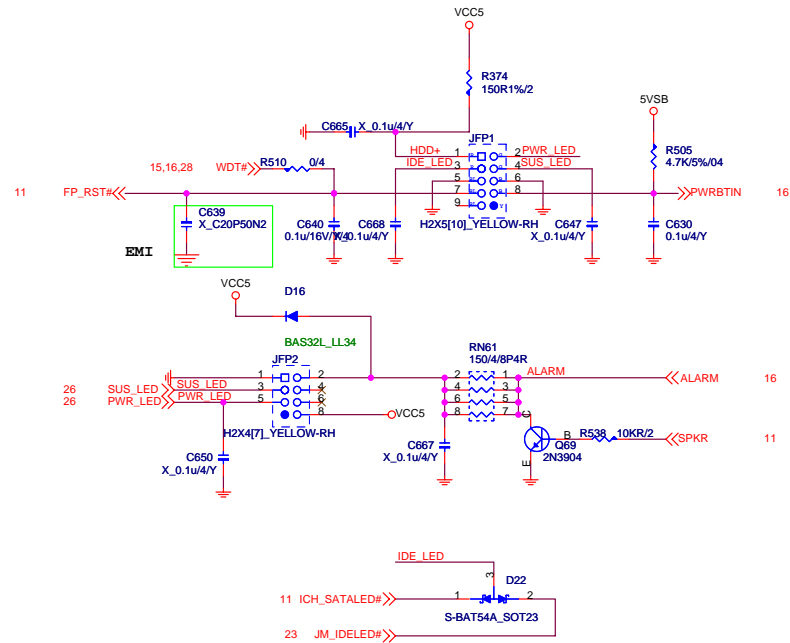


Place in bottom

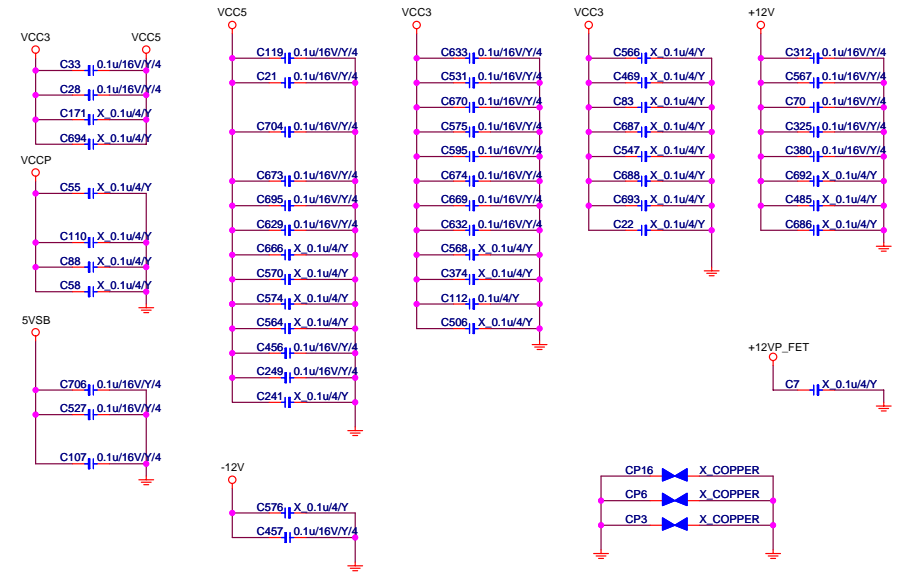
ATX POWER CONNECTOR



FRONT PANNEL



Cap. for EMI & Power



			MICRO-STAR INT'L CO.,LTD	
			MS-7365	
Size Custom	Document Description ATX PWR-Connector & Front Panel			Rev 0A
Date: Monday, April 02, 2007		Sheet 29 of 34		

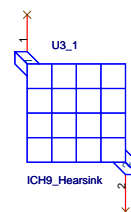
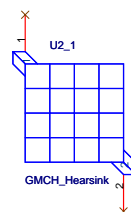
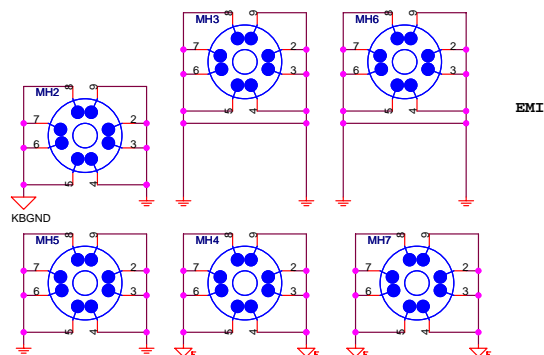
Optical Fiducial Marks-120



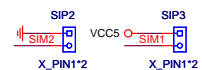
Optical Fiducial Marks-100



Mounting Holes



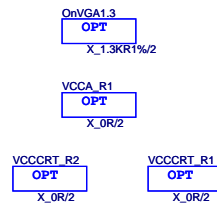
Simulation



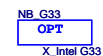
USB Connector for non 1394



Resistor for P35/G33 of VGA Part



For G33



For ICH9R



LGA775-CPU		
0.8375V - 1.6000V Core	-	125A
1.2V FSB Vtt	-	4.6A

Bearlake-G (G33)		
1.2V FSB_VTT	-	1.2 A
1.25V Core	-	13.8A
1.25V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.3A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	4.9A

ICH9		
1.05V Core	-	1.16A
1.25V DMI	-	41 mA
1.2V FSB_VTT	-	2 mA
1.5V_A USB/SATA/PLL	-	1.65A
1.5V_B PCI Exp.	-	0.65A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

1394 Controller VT6308		
3.3V	-	156mA

HD Audio STAC9227		
3.3V AUDIO	-	32mA
5V AUDIO	-	200mA

CK505		
3.3V VDD_48/PCI/REF	-	250mA
0.3V - 1V CPU/SRC/DOT/PLL	-	80mA

RTL8111B		
3.3V_SB I/O & LED	-	668mA
1.8V EVDD/AVDD	-	198mA
1.5V VDD	-	367mA

ISL6306		
VCCP VRD11/10.x	-	0.8375V-1.6000V
4-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

uP6103 SW-Power		
VCC_DDR	-	1.5V PWM 18.64A

uP6103 SW-Power		
V_1P25_CORE	-	1.25V PWM 21.21A

MS12 Controller		
V_1P05_ICH	-	1.05V Linear 1.16A
V_FSB_VTT	-	1.2V Linear 5.8A
V_1P5_ICH (T0263)	-	1.5V Linear 2.31A
VCC3_SB	-	3.3V Linear 2.5A
5VDUAL1	-	5V Switch 6.35A
5VDIMM	-	5V Switch 6.99A

DDRIII x4 & TERMINATOR		
0.9V VTT_DDR	-	0.83A
1.5V VCC_DDR (S0,S1)	-	7.2A

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI Express x 1 slot		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI Express x 4 slot		
+12V	-	5.5A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x2		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB x12		
+5V (S0,S1)	-	6.0A
+5V (S3)	-	20mA


PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAudio		
+5VR	-	500mA

+12V		
ATX 2x2	-	

+5V	+3.3V	+5VSB	+12V
24.97A			
ATX POWER			

■ Bead or Inductor
 ✕ X-Copper

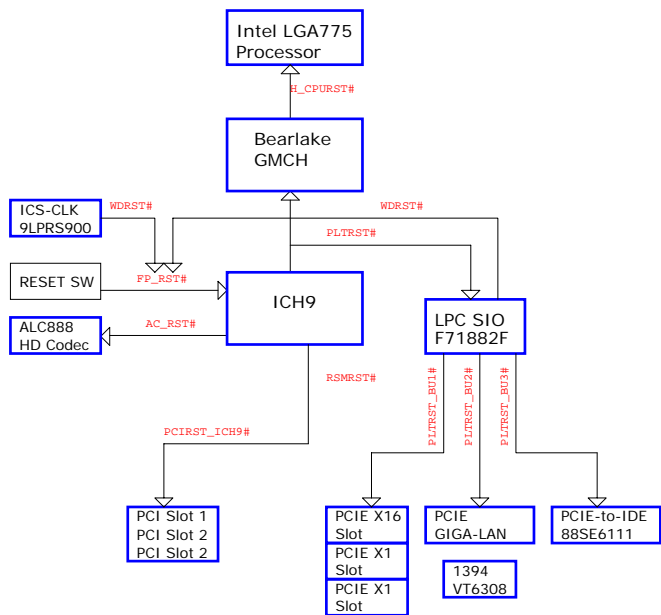


MICRO-STAR INT'L CO.,LTD

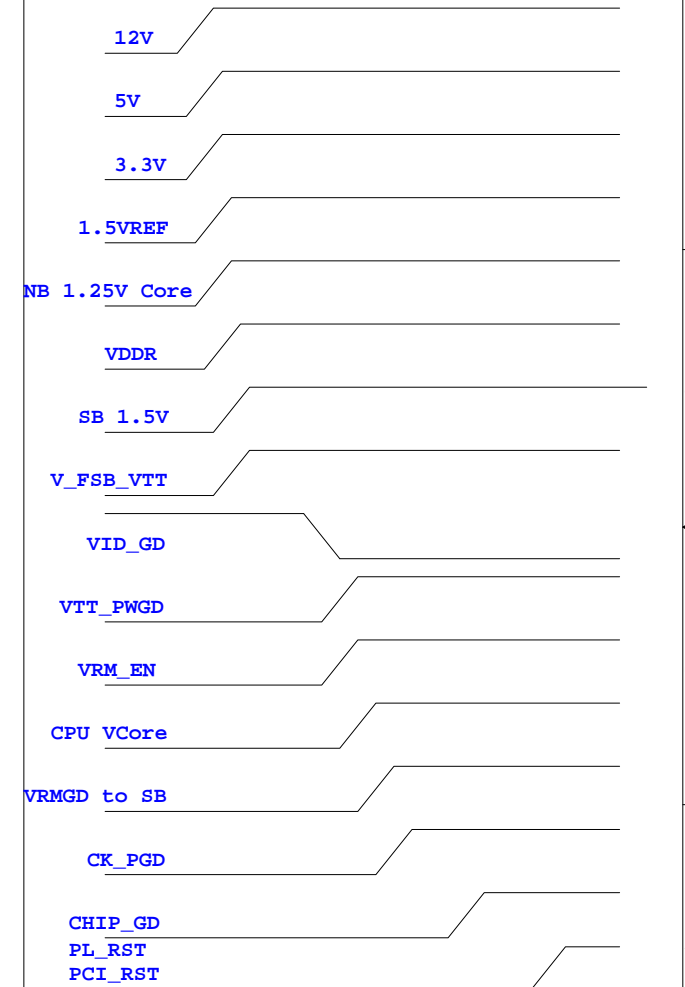
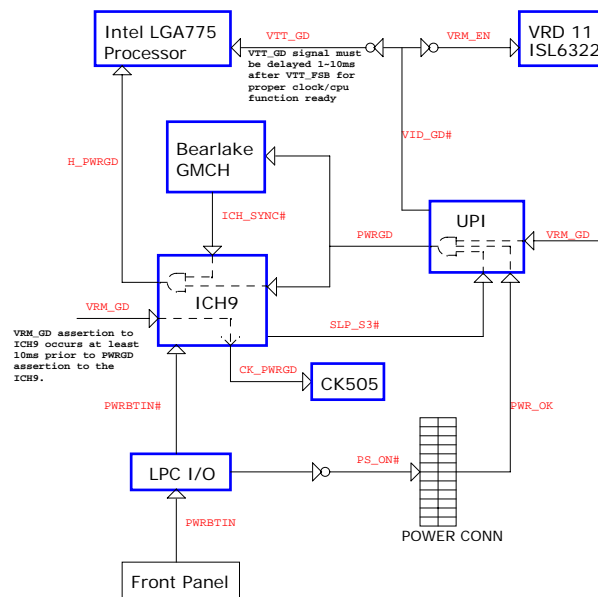
MS-7365

Size Custom	Document Description Power Delivery	Rev 0A
Date: Monday, April 02, 2007		Sheet 31 of 34

RESET MAP



PWROK MAP



ICH8

GPIO	Alt Func	I/O/NC	Power	ToI	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2/3_FANTAC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
-------	-------------	------------

SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	P/N_DDR0_A P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394



MICRO-STAR INT'L CO.,LTD		
MS-7365		
Size Custom	Document Description GPIO setting & PCI Routing	Rev 0A
Date: Monday, April 02, 2007		
Sheet 33 of 34		

- 0A
1. Change COM1's PartNO 0131-A
 2. Remove R452 、 R630 0131-D
 3. Change JSPD1 to 3 Pins PartNO 0131-D
 4. Change R299's PartNO 0131-D
 5. Change DDR II Termination Resistor to 56 ohm 0208
 6. Remove C1014 0208
 7. Change JAUD1 's PartNO 0208
- D
- 1.0
1. Change RTC circuit (JBAT pin1 change to NC) P11 0313
 2. Change VRM(change 3coppers to R1006、 1011、 1019) P28 0313
 3. Change PowerOK's sequence (use ICH_VRM_PGD) P26 0313
 4. Add R1021.1027.1029.1031 on the Gate P27 0313
 5. Add L39.40.41 on VGA for EMI. P17 0313
 6. Add R644 for EMI. P20 0313
 7. Change Smart FAN to SIO P18 0313
 8. Change RN33 to 47ohm; P15 0313
 9. Change USB's 0ohm RN 0315
 10. Add DDR2_DET# 0316
 11. Delete C490, C293, C712, C1039, C29, C1030 0319
 12. Change CN2 to 15pF 0321
 13. Change CN2 to 22pF 0323
 14. DDR II Termination change to 68ohm 0329
 15. R401\R419 change to 20K,R210 chagne to 1K 0329
 16. C404 change from 0.01uF to 0.1uF ,C231、 C572、 C63、 C235=NC 0329
 17. C74=1uF, R200=2K, R5 = NC 0329
 18. Change CPU GTLREF 'voltage divider to 0.635 0330
 19. Reserve RN23\53\54\55\63\66 for USB 0331
 20. Change GMCH_HEATSINK to E31-0402370-K08 0402
- C
- ff
- B
- A